REMARKS

This responds to the Office Action mailed on December 30, 2004.

Claims 1-4, 9-12, and 14-20 are amended, claims 5-8, 13, 21 and 22 are canceled, and claims 23-29 are added; as a result, claims 1-4, 9-12, 14-20, and 23-29 are now pending in this application.

Newly Added Claims

Applicant has added claims 23-29.

Support for claims 23, 27, and 29 can be found in the Instant Application at least at page 9, lines 3-6, and 14-16, page 7, line 18-22.

Support for claims 24 and 28 can be found in the Instant Application at least at page 6, lines 11 and 12.

Support for claim 25 can be found in the Instant Application at least at page 7, lines 23-25.

Support for claim 26 can be found in the Instant Application at least at page 6, line31 – page 7, line 3.

§103 Rejection of the Claims

Claims 1-19 and 21 were rejected under 35 USC § 103(a) as being unpatentable over Ozeki et al. (U.S. 5,402,385) in view of Helmbold et al. (U.S. 5,497,450). Applicant respectfully traverses this rejection because the Office Action has not established a *prima facie* case of obviousness.

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *M.P.E.P.* § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir. 1991)).

Applicant respectfully submits that the Office Action does not establish a *prima facie* case of obviousness because the references do not teach or suggest all the claim elements, and even if they did, there is no suggestion or motivation to combine the references.

THE REFERENCES DO NOT TEACH OR SUGGEST ALL THE CLAIM ELEMENTS

Discussion of Claim 1

Claim 1 recites "if the selected address matches an address of the data register, disabling at least one of the one or more load conditions of the data register." In rejecting claim 1, the Office Action admits, "Ozeki et al does not disclose disabling the load condition as claimed." However, the Office Action asserts that Helmbold discloses this claim feature at column 8, lines 21-36. See Office Action at Page 2, Number 2, Letter a. The cited passage from Helmbold states:

> The memory protection circuit 36 includes a protection limits register 160 into which is written the high limit of the address range to be protected and the lower limit of the address range to be protected. The address of the RAM 16 that is being written to is compared to the high limit value and to the low limit value by respective comparators 162 and 164 to determine whether the write address is within the protected address range. If it is not, that address of the RAM 16 may be written to. However, if the write address is within the protected address range, the memory protection circuit 36 blocks the write signal so as to prevent the protected area of the RAM from being written to. Helmbold at col 8, lines 21-36.

Applicant respectfully submits that the Office Action has mischaracterized Helmbold. This passage describes a memory protection circuit for protecting areas of RAM by writing high and low limits of a protected address range to "protection limits registers." However, this passage does not mention *load conditions of a data register*, much less teach or suggest the claimed "disabling at least one of the one or more load conditions of the data register." Emphasis added. According to this passage, the memory protection circuit loads a protection limits register to prevent writing to protected areas of *RAM*, but does not disable load conditions of any register. Therefore, the combination of Ozeki and Helmbold does not teach or suggest each and every element of claim 1.

Discussion of Claims 9 and 14

Independent claims 9 and 14 each include features similar to those noted in the discussion of independent claim 1. For at least the reasons noted above, Applicant respectfully submits that the combination of Ozeki and Helmbold does not teach or suggest each and every element of dependent claims 9 and 14.

Discussion of Claims 2-4, 10-12, and 15-20

Claims 2-4, 10-12, and 15-20 each depend, directly or indirectly, on one of independent claims 1, 9 or 14. For at least the reasons noted above, Applicant submits that the combination of Ozeki and Helmbold does not teach or suggest every element of dependent claims 2-4, 10-12, and 15-20.

Discussion of Claims 5-8, 13 and 22

Applicant has canceled claims 5-8, 13, and 22.

Discussion of Claim 20

Claim 20 was rejected under 35 USC § 103(a) as being unpatentable over Ozeki et al. in view of Helmbold et al. and Kimura (U.S. 5,625,593). Claim 20 depends on independent claim 1, and as such, includes all of the features of independent claim 1. As noted above, Applicant submits that the combination of Ozeki and Helmbold does not teach or suggest each and every element of dependent claim 20. For the combination of Ozeki, Helmbold and Kimura to teach or suggest each and every element of dependent claim 20, Kimura must teach or suggest what Ozeki and Helmbold are missing. The Office Action does not point to and Applicant cannot find any passage in Kimura that teaches the claimed "disabling at least one of the one or more load conditions of the data register." Therefore, Applicant respectfully submits that the combination of Ozeki, Helmbold and Kimura does not teach or suggest each and every element of dependent claim 20.

THERE IS NO SUGGESTION TO COMBINE OZEKI AND HELMBOLD

The Office Action has improperly combined Ozeki with Helmbold. For a proper combination, the Office Action must show that some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art would lead an individual to combine the relevant teaching of the references. *In re Fine,* F.2d 1071, 1074, 5 USPW2d 1596, 1598 (Fed. Cir. 1988).

The *Fine* court stated,

> Obviousness is tested by "what the combined teaching of the references would have suggested to those of ordinary skill in the art." *In re Keller*, 642 F.2d 413, 425, 208 USPQ 871, 878 (CCPA 1981)). But it "cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination." *ACS Hosp. Sys.*, 732 F.2d at 1577, 221 USPQ at 933. And "teachings of references can be combined *only* if there is some suggestion or incentive to do so." *Id.* (emphasis in original).

Ozeki describes techniques for write protecting a memory card of a gaming machine, whereas Helmbold teaches using a printer memory protection circuit to write protect a range of RAM addresses. The Office Action asserts that "it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the step of disabling the load condition of Helmbold to the write protecting method of Ozeki in order to protect the protected data." Office Action at pages 2 and 3. However, this assertion is unfounded, as the Office Action does not identify a single passage in any of the references that teaches or suggests combining Ozeki with Helmbold. Because there is no teaching or suggestion to combine the cited references, Applicant submits that the combination is improper. As such, Applicant requests withdrawal of the rejections under 35 USC §103.

Correction

In Applicant's response to the Office Action mailed November 14, 2003, Applicant incorrectly stated, "Applicant would agree that Helmbold discloses disabling one loading condition of the data register under the specific condition of 'if the selected address matches of the data register' then the memory protection circuit 36 blocks the write signal so as to prevent

the protected area of RAM being written to. (Col 8, lines 21-37)." Response to Office Action that was mailed 11/14/03 at Page 6, Paragraph 3. After further review, Applicant does **not** believe Helmbold discloses these concepts. As noted above, Helmbold describes a memory protection circuit for protecting areas of RAM by writing high and low limits of a protected address range to "protection limits registers." However, Helmbold does not mention *load conditions of a data register*, much less teach or suggest the claimed "disabling at least one of the one or more load conditions of the data register." Emphasis added. According to Helmbold, the memory protection circuit loads a protection limits register to prevent writing to protected areas of *RAM*, but does not disable load conditions of any register.

Reservation of Rights

Applicants do not admit that documents cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such documents should not be construed as admissions that the documents are prior art. Applicants also reserve the right to pursue cancelled and originally filed claims in a continuation application. Furthermore, Applicants do not acquiesce to any of the Examiner's assertions about the claims or the cited references and reserves the right to argue these assertions in the future.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney 773.961.1480 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account 502596.

Respectfully submitted,

STEPHEN A. CANTERBURY

By his Representatives,

WMS Gaming Inc.
3401 N. California Ave.
Chicago, IL 60618
773.961.1480

Date 3/31/05

By Michael Blankstein
Michael Blankstein
Reg. No. 37,097

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 31st day of March, 2005.

Pamela Lowenthal
Name

Signature